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An Insight on RF Performances Of Gate Metal Work Function Engineered Hetero-Gate Dielectric TFET

Deepak Sigroha[1*], Rajesh Kumar Pathak[2] and Kuldip Singh[2]

[*1]Department of Electronics Engineering, Rajkiya Engineering College Sonbhadra, Uttar Pradesh-231206, India.

[2] Department of Electronics & Communication Engineering, Sant Longowal Institute of Engineering & Technology (Deemed to be University), Punjab-148106, India.

[*1]Corresponding Author: Deepak Sigroha

Abstract

This paper presents novel hetero-gate TFET architecture to improve the DC and RF characteristics of the device. To analyze the improved functionality, here we compared the proposed TFET with the conventional TFET. The RF parameters such as gate-to-gate capacitance (C_{gg}), gate-to-drain capacitance (C_{gd}), gate-to-source capacitance (C_{gs}), transconductance (g_m), cut-off frequency (f_T), and gain bandwidth product (GBP) are analyzed for both of the TFETs. The effects of scaling of oxide thicknesses on the transfer characteristics are also studied for the proposed TFET.

Keywords: Band gap narrowing model, Hetero-gate dielectric, Transconductance, RF parameters

1 Introduction

To fulfill present semiconductor demands, the dimensions of devices are continuously scaled down, which causes various short channel effects (SCEs) [1-10], high off-current (I_{OFF}), and less on drain current (I_{ON}) [11]. At room temperature, the SS value of MOSFET is limited to 60 mV/decade [11-12]. Due to the drift-diffusion phenomenon of MOSFET, no techniques can lower the limit of SS (60 mV/decade) [13]. Therefore, an alternative device has been looked out for, which not only shows high I_{ON}, less I_{OFF}, but also offers a steep subthreshold slope. One of the most acceptable alternative devices is a TFET device, which shows very less leakage current [14-16] and SS below 60 mV/dec. In TFET, the tunneling mechanism provides better immunity over SCEs [17]. To increase the device's functionality, a variety of other TFET topologies have been proposed such as DG TFET [18], triple material DG TFET [19], DG with source pocket TFET [20], and heterojunction TFETs [21-23], etc.

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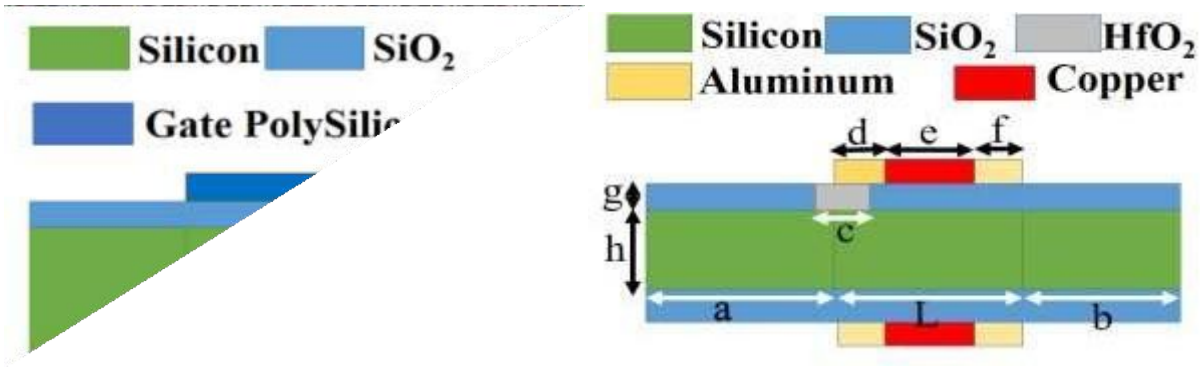
In the concern of creating a steep band profile at the source/channel interface and improving RF performances, a DG TFET is proposed with a modification in the gate oxide region and the gate region. This paper has many sections: In section II, we describe the architecture of the proposed TFET with details of the dimensions of the parameters used during the extraction of results. In Section III, the results of the extracted DC and RF parameters. Finally, in the last Section IV, we conclude the presented work.

2 Device Simulation Deck

The 2-D schematic of the conventional and proposed TFET is shown in Figure 1. In the proposed TFET, Silicon (Si) material is used as a semiconductor material. Above the Si semiconductor, SiO_2 (k=3.9) is used as a dielectric material except that HfO_2 (k=22) is used above the source-channel junction. The combination of SiO_2 and HfO_2 gate dielectric is hetero-gate dielectric. The gate materials such as Aluminum (ϕ_m= 4.1 eV) and Copper (ϕ_m= 4.7 eV) are used above the oxide layer. The Aluminum gate material is used near the source and the drain whereas Copper is used in between Aluminum. The source and drain each has a doping concentration of $6 \times 10^{20}cm^{-3}$ and $5 \times 10^{20}cm^{-3}$ and the channel has $3 \times 10^{16}cm^{-3}$. The dimensions of the dimensional parameters (Figure 1) are listed in Table I.

The simulation of the proposed TFET and the results are extracted using Synopsys TCAD [24]. Since the tunneling mechanism exists in the TFET device, the non-local band-to-band tunneling (BTBT) model is used. Moreover, band gap narrowing, SRH recombination, Fermi-Dirac statistics, and doping-dependent mobility models are used [24].



(a) (b)

Figure 1. 2-D structure of (a) Conventional and (b) Proposed TFET

3 Simulation Results and Discussion

This section includes firstly, the DC transfer properties of the proposed TFET versus the traditional TFET. Further, the simulated RF parameters are extracted and analyzed for conventional and proposed devices.

Table I: Dimensions of Figure 1

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Parameters	Value(nm)	
	Conventional TFET	Proposed TFET
a	100	100
b	100	100
c	0	4
d	0	15
e	0	20
f	0	15
g	1	1
h	10	10
L	50	50

3.1 Comparative analysis of I_D-V_{GS} curve of proposed and the conventional TFET

The I_D-V_{GS} curve of the conventional and the proposed TFET is shown in Figure 2. As observed from Figure 2, the proposed TFET shows improved characteristics compared to the conventional TFET. The improved characteristics of the proposed TFET can be explained by its architecture. The presence of high-k dielectric in the tunneling region increases the gate capacitive effect which in turn increases the electric field at the source-channel interface and thus helps in achieving a higher tunneling rate of electrons. The higher tunneling rate of electrons causes a higher ON-state current. Adding to it, the presence of low ϕ_m gate material towards the source side, the flat band voltage between the gate material towards the source side and the semiconductor decreases compared to the flat band voltages of gate material copper and the semiconductor. The lower value of flat band voltage pushes the band downward in the source region and reduces the barrier width and hence increases the tunneling rate. In the proposed TFET, the greater electron tunneling rate at the source channel junction increases the electron current density.

Transconductance (g_m) is an essential design parameter for low-power digital circuit applications. mathematically, g_m can be expressed as [25]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

The efficiency of the device can be directly measured from the $\frac{g_m}{I_D}$. The higher value of $\frac{g_m}{I_D}$, the better the ability of TFET to act as a potential energy-saving device. The plots of Figure 3 follow the plots of Figure 2. The higher value of g_m of the proposed TFET shows a more efficient device than conventional TFET.

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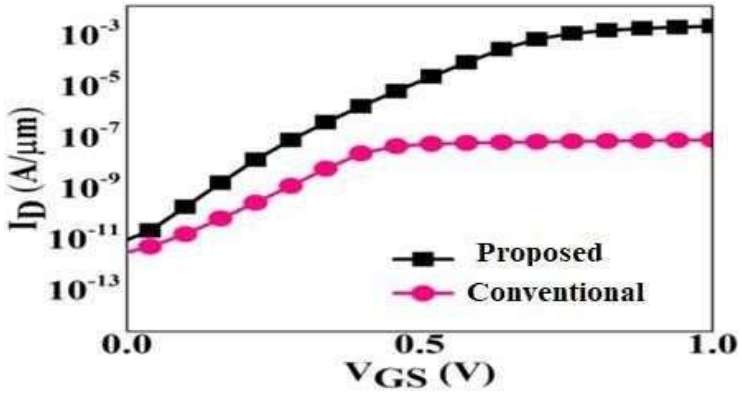

Figure 2. The plot of I_D-V_{GS} for conventional and proposed TFET with V_{DS}=0.5 V

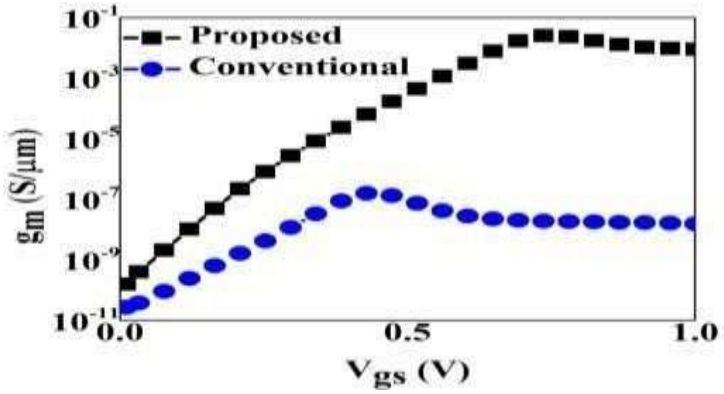

Figure 3. g_m versus V_{GS} curve for both TFETs with V_{DS}=0.5 V

3.2 Comparison of RF parameters for both devices

The RF performances of the device are analyzed by extracting some of the significant RF parameters such as C_{gd}, C_{gs}, C_{gg}, f_T, and GBP.

The capacitances C_{gd} and C_{gg}, decide the device's performance [26]. Figures 4 and 5 show the C_{gd} and C_{gg} against gate voltage (V_{GS}) for the proposed and conventional TFET. It is evident from the plots that the values of gate capacitances (C_{gd} and C_{gg}) are less for the proposed device as compared to the conventional device. This is because of the modification in the device, i.e. the presence of low ϕ_m gate material and the low-k material at the drain side. Due to the low-k material, the coupling reduces between the gate and drain point, whereas the depletion width at the drain-channel junction increases because of the low work function metal gate. An opposite behavior is noticed in Figure 6 that C_{gs} is more for the modeled TFET as compared to the traditional device. The more value of C_{gs} defines the more influence of gate control over the channel and thus, more coupling of the gate and the source.

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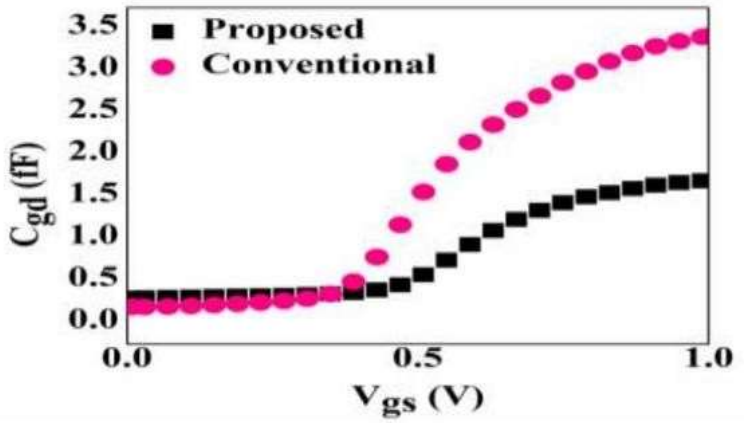

Figure 4. The plot of C_{gd}-V_{GS} for both TFETs with V_{DS}=0.5 V

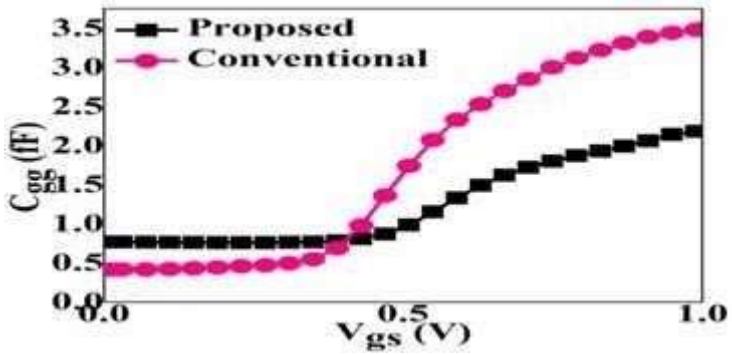

Figure 5. The plot of gate-to-gate capacitance for both TFETs with V_{DS}=0.5 V

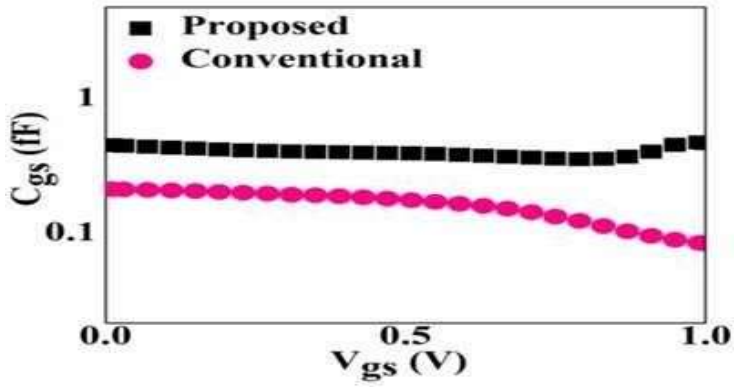

Figure 6. C_{gs} versus V_{gS} for both TFET with V_{DS}=0.5 V

Figure 7 shows the f_T -V_{GS} curve for both devices. For RF response, f_T is an important parameter. It is the working frequency of the device in which the short circuit current gain decreases up to unity. Mathematically, the equation of f_T is written as [26]

$$f_T = \frac{g_m}{2\pi(C_{gd}+C_{gs})}$$

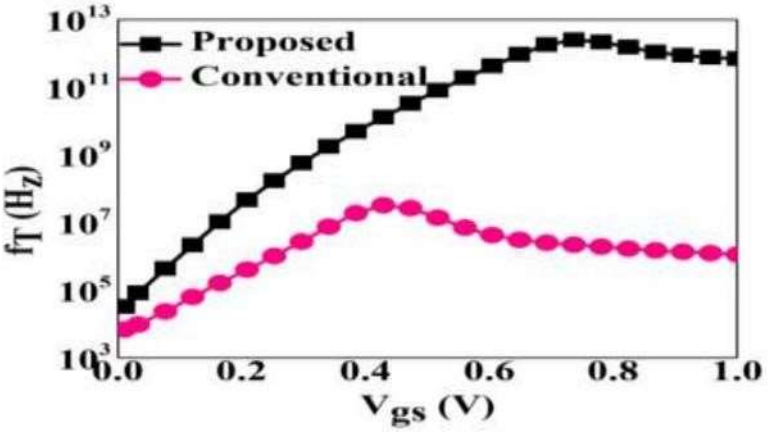

Figure 7. Cut-off frequency (f_T) versus V_{GS} for both TFET

It is observed from Figure 7 that initially f_T increases up to some extent of V_{GS} and then decreases for both of the devices. From the starting point, f_T increases due to increases in transconductance (Figure 3) and the falling nature of the curves is due to the reduction of transconductance and the combined effect of increased C_{gd}, irrespective of both of the devices. The higher value of f_T is found for the proposed device because the gate material has low ϕ_m and the low-k dielectric lowers the value of C_{gd}. Whereas, the low ϕ_m gate material and the high-k dielectric at the tunnel junction enhance the value gm. Thus, the higher f_T is obtained for the proposed TFET due to the combined effect of C_{gd} and g_m.

Lastly, one of the most significant RF parameters of the device, gain bandwidth product (GBP) is shown in Figure 8. The GBP equation can be written as [26]

$$GBP = \frac{g_m}{20\pi C_{gd}}$$

From Figure 8, it can be seen that GBP is higher for the proposed device. The improved behavior of GBP can be explained by the above-mentioned expression of GBP. The smaller value of C_{gd} and the higher value of g_m enhance the behavior of GBP in case of proposed device.

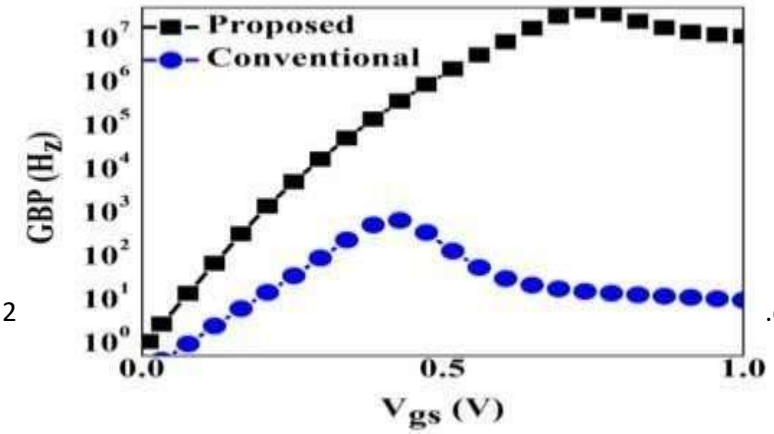

Figure 8. Variation in GBP with V_{GS} for both TFET with V_{DS}=0.5 V

3.3 Analysis of effects of scaling of oxide thicknesses

As the proposed TFET shows improved performance compared to conventional TFET, further analysis is carried on by varying the oxide thicknesses (t_{ox}) of the oxide material. The transfer characteristics for different t_{ox} are plotted in figure 9. From the plot, it can be computed that with the increasing t_{ox}, I_D decreases. As the t_{ox} increases (decreases), the gate capacitive effect decreases (increases). The degrading (enhancing) behavior of gate capacitance decreases (increases) the drain current.

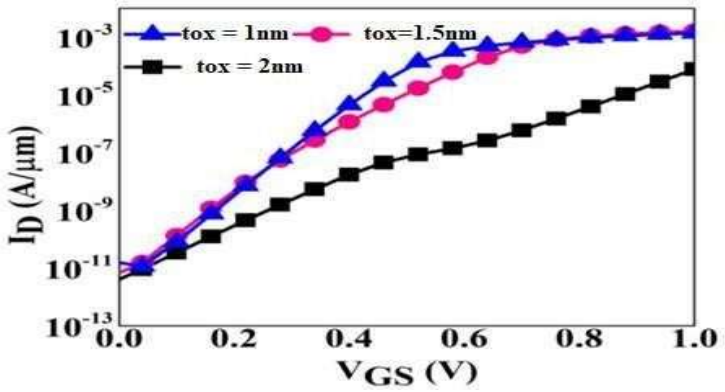

Figure 9. I_D-V_{GS} for different t_{ox} of the proposed TFET with V_{DS}=0.5 V

4 Conclusions

From the above analysis, the proposed TFET enhances the electrical characteristics in terms of I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, and SS. The presence of low ϕ_m gate material and the high-k dielectric in the source-channel tunnel junction enhances the drain current, as the higher electric field creates abruptness in the source-channel junction. whereas, the presence of low ϕ_m gate material in the drain side degrades the value of gate-drain capacitances, and hence, improved RF performances are found. Therefore, the improved RF behavior makes the proposed device useful for low-power RF circuit applications.

5 Abbreviations

TFET: tunnel field effect transistor; RF: radio frequency; GBP: gain bandwidth product; SCEs: short channel effects; SS: subthreshold swing; DG: double gate; BTBT: band to band tunneling; SRH: Shockley Read Hall.

References

[1] V. M. Srivastava, "Scaling effect of cylindrical surrounding double-gate MOSFET: A device beyond 22 nm technology," 2017 4th International Conference on Advanced Computing and Communication Systems (ICACCS), Coimbatore, 2017, pp. 1-5.

[2] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, G. Pananakakis and G. Ghibaudo," Semianalytical Modeling of Short-Channel Effects in Lightly Doped Silicon Trigate MOSFETs," in IEEE Transactions on Electron Devices, vol. 55, no. 10, pp. 2623-2631, Oct. 2008.

[3] S. Bangsaruntip, G. M. Cohen, A. Majumdar and J. W. Sleight, "Universality of Short-Channel Effects in Undoped-Body Silicon Nanowire MOSFETs," in IEEE Electron Device Letters, vol. 31, no. 9, pp. 903-905, Sept. 2010.

[4] S. E. Hosseini, M. K. Anvarifard and M. G. Armaki, "Two-Dimensional Analytical Modeling of Fully Depleted Short-Channel DG SOI MOSFET," 2009 International Conference on Signal Processing Systems, Singapore, 2009, pp. 897-900. Processing Systems, Singapore, 2009, pp. 897-900.

[5] M. Khani Parashkoh, S. E. Hosseini and I. Abaspur Kazerouni, "Reducing short channel effects in dual gate SOI-MOSFETs with a drain dependent gate bias," 2010 18th Iranian Conference on Electrical Engineering, Isfahan, 2010, pp. 372-376.

[6] S. Sleva and Y. Taur, "The influence of source and drain junction depth on the short-channel effect in MOSFETs," in IEEE Transactions on Electron Devices, vol. 52, no. 12, pp. 2814-2816, Dec. 2005.

[7] A. I. Khan, M. K. Ashraf and A. Haque, "Influence of wave function penetration on short channel effects in nanoscale double gate MOSFETs," 2007 IEEE Conference on Electron Devices and Solid-State Circuits, Tainan, 2007, pp. 109-112.

[8] M. J. Kumar and M. Siva, "The Ground Plane in Buried Oxide for Controlling Short-Channel Effects in Nanoscale SOI MOSFETs," in IEEE Transactions on Electron Devices, vol. 55, no. 6, pp. 1554-1557, June 2008.

[9] Chun-Hsing Shih, Yi-Min Chen and Chenhsin Lien, "Effect of insulated shallow extension for the improved short-channel effect of sub-100 nm MOSFET," International Semiconductor Device Research Symposium, 2003, Washington, DC, USA, 2003, pp. 158-159.

[10] J. E. Suseno, M. A. Riyadi, and R. Ismail, "Short channel effect of SOI vertical sidewall MOSFET," 2008 IEEE International Conference on Semiconductor Electronics, Johor Bahru, 2008, pp. 487-490.

[11] W. Y. Choi, B. Park, J. D. Lee and T. K. Liu, "Tunneling Field-Effect Transistors (TFETs) with Subthreshold Swing (SS) less than 60 mV/dec," in IEEE Electron Device Letters, vol. 28, no. 8, pp. 743-745, Aug. 2007.

[12] T. Krishnamohan, D. Kim, S. Raghunathan and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and <60mV/dec subthreshold slope," 2008 IEEE International Electron Devices Meeting, San Francisco, CA, 2008, pp. 1-3.

[13] D. Soni, D. Sharma, S. Yadav, M. Aslam, D. S. Yadav and N. Sharma, "Gate Metal Work Function Engineering for the Improvement of Electrostatic Behaviour of Doped Tunnel Field Effect Transistor," 2017 IEEE International Symposium on Nanoelectronics and Information Systems (iNIS), Bhopal, 2017, pp. 190-194.

[14] M. J. Lee and W. Y. Choi, "Effects of Device Geometry on Hetero-Gate-Dielectric Tunneling Field-Effect Transistors," in IEEE Electron Device Letters, vol. 33, no. 10, pp. 1459-1461, Oct. 2012.

[15] H. Wang et al., "A Novel Barrier Controlled Tunnel FET," in IEEE Electron Device Letters, vol. 35, no. 7, pp. 798-800, July 2014.

[16] A. Revelant, P. Palestri, P. Osgnach, L. Selmi, “Calibrated multi-subband Monte Carlo modeling of tunnel-FETs in silicon and III–V channel materials,” Solid-State Electronics, vol. 88, pp. 54-60, 2013.

[17] L. Lattanzio, N. Dagtekin, L. De Michielis, and A. M. Ionescu, "On the Static and Dynamic Behavior of the Germanium Electron-Hole Bilayer Tunnel FET," in IEEE Transactions on Electron Devices, vol. 59, no. 11, pp. 2932-2938, Nov. 2012.

[18] D. Gupta, N. Bagga, and S. Dasgupta, "Reduced Gate Capacitance of Dual Metal Double Gate Over Single Metal Double Gate Tunnel FET: A Comparative Study," 2018 Conference on Emerging Devices and Smart Systems (ICEDSS), Tiruchengode, 2018, pp. 110-112.

[19] S. Safa, S. L. Noor and M. Z. R. Khan, "Triple material double gate TFET with optimized Si film thickness," 2016 3rd International Conference on Electrical Engineering and Information Communication Technology (ICEEICT), Dhaka, 2016, pp. 1-4.

[20] Z. Yu, Y. Dong, X. Lin and L. Zhang, "Current enhanced double-gate TFET with source pocket and asymmetric gate oxide," 2016 IEEE International Nanoelectronics Conference (INEC), Chengdu, 2016, pp. 1-2.

[21] H. Lin and V. P. Hu, "Device design of vertical nanowire III-V heterojunction TFETs for performance enhancement," 2018 7th International Symposium on Next Generation Electronics (ISNE), Taipei, 2018, pp. 1-4.

[22] U. E. Avci and I. A. Young, "Heterojunction TFET Scaling and resonant-TFET for steep subthreshold slope at sub-9nm gate-length," 2013 IEEE International Electron Devices Meeting, Washington, DC, 2013, pp. 4.3.1-4.3.4.

[23] G. S. Sangeetha, T. E. A. Khan, and T. A. S. Hameed, "SiGe/Si heterojunction TFET for analog signal applications," 2016 International Conference on Next Generation Intelligent Systems (ICNGIS), Kottayam, 2016, pp. 1-6.

[24] Sentaurus Device User, Synopsys, 2009, p. 2009.

[25] Rajashree Das, Rupam Goswami, Srimanta Baishya, “Tri-gate heterojunction SOI Ge-FinFETs,” Superlattices and Microstructures, vol. 91, pp. 51-61, 2016.

[26] D. Soni, D. Sharma, S. Yadav, M. Aslam, D. S. Yadav and N. Sharma, "Gate Metal Work Function Engineering for the improvement of Electrostatic Behaviour of Doped Tunnel Field

Effect Transistor," 2017 IEEE International Symposium on Nanoelectronics and Information Systems (iNIS), Bhopal, 2017, pp. 190-194.